

**PATENT APPLICATION**

Sheet 1 of 5

<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	<b>ATTY. DOCKET NO.</b> 200209677-1	<b>APPLICATION NO.</b> 10/759867	<b>CONFIRMATION NO.</b>
<b>APPLICANT</b> Elias Gedamu			
<b>FILING DATE</b> 1/15/2004		<b>GROUP</b> 2825	

**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
SM	1A	6,571,359	5/27/2003	Padwekar et al.	
SM	1B	6,523,151	2/18/2003	Hekmatpour	
SM	1C	6,484,275	11/19/2002	Josephson et al.	
SM	1D	6,430,705	8/6/2002	Wisor et al.	
SM	1E	6,427,224	7/30/2002	Devins et al.	
SM	1F	6,427,216	7/30/2002	El-Kik et al.	
SM	1G	6,385,740	5/7/2002	Treadway et al.	
SM	1H	6,385,552	5/7/2002	Snyder	
SM	1I	6,370,658	4/9/2002	Jeong	
SM	1J	6,363,509	3/26/2002	Parulkar et al.	
SM	1K	6,285,974	9/4/2001	Mandyam et al.	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

SM	1Q	Chen, Li and Sujit Dey, "Software-Based Self-Testing Methodology for Processor Cores," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 3, March 2001 (pages 369-380).
SM	1R	Chen, Li, Sujit Dey, Pablo Sanchez, Krishna Sekar, and Ying Chen, "Embedded Hardware and Software Self-Testing Methodologies for Processor Cores," Los Angeles, CA, 2000 (6 pages).
SM	1S	Geotest, "Dynamic Testing of Micro-Processor Based Products," Santa Ana, CA (4 pages).

<b>EXAMINER</b> Suresh Memula	<b>DATE CONSIDERED</b> 3/10/2006
----------------------------------	-------------------------------------

PATENT APPLICATION

Sheet 2 of 5

<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200209677-1	10/39867	
	APPLICANT		
	Elias Gedamu		
	FILING DATE	GROUP	
	1/15/2004	2825	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
SM	2A	6,212,667	4/3/2001	Geer et al.	
SM	2B	6,181,004	1/30/2001	Koontz et al.	
SM	2C	6,064,948	5/16/2000	West et al.	
SM	2D	6,055,649	4/25/2000	Deao et al.	
SM	2E	6,042,384	3/28/2000	Loiacono	
SM	2F	6,031,992	2/29/2000	Cmelik et al.	
SM	2G	6,028,983	2/22/2000	Jaber	
SM	2H	5,928,334	7/27/1999	Mandyam et al.	
SM	2I	5,884,023	3/16/1999	Swoboda et al.	
SM	2J	5,867,719	2/2/1999	Harris, II et al.	
SM	2K	5,862,366	1/19/1999	Schmidt et al.	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L				
	2M				
	2N				
	2O				
	2P				

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

SM	2Q	Johnson, David J. C., "HP's Mako Processor," Fort Collins, CO, October 2001 (16 pages).
SM	2R	Kranitis, N., A. Paschalis, D. Gizopoulos, and Y. Zorian, "Effective Software Self-Test Methodology for Processor Cores" (6 pages).
SM	2S	Kranitis, N., G. Xenoulis, D. Gizopoulos, A. Paschalis, and Y. Zorian, "Low-Cost Software-Based Self-Testing of RISC Processor Cores," 2003 (6 pages).

EXAMINER	DATE CONSIDERED
Suresh Memula	3/10/2006

**PATENT APPLICATION**

Sheet 3 of 5

<b>FORM PTO-1449</b>  <b>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</b>  (Use several sheets if necessary)	<b>ATTY. DOCKET NO.</b> 200209677-1	<b>APPLICATION NO.</b> 10/759867	<b>CONFIRMATION NO.</b>
<b>APPLICANT</b> Elias Gedamu			
<b>FILING DATE</b> 1/15/2004		<b>GROUP</b> 2825	

**REFERENCE DESIGNATION U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
SM	3A	5,841,968	11/24/1998	Caldera et al.	
SM	3B	5,699,506	12/16/1997	Phillips et al.	
SM	3C	5,673,274	9/30/1997	Yoshida	
SM	3D	5,673,272	9/30/1997	Proskauer et al.	
SM	3E	5,671,531	9/30/1997	Mugiya	
SM	3F	5,654,972	8/5/1997	Kuroiwa et al.	
SM	3G	5,638,382	6/10/1997	Krick et al.	
SM	3H	5,623,499	4/22/1997	Ko et al.	
SM	3I	5,617,531	4/1/1997	Crouch et al.	
SM	3J	5,596,583	1/21/1997	Krenik et al.	
SM	3K	5,590,134	12/31/1996	Yin	

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

**OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)**

SM	3Q	Lai, Wei-Cheng and Kwang-Ting Cheng, "Instruction-Level DFT for Testing Processor and IP Cores in System-on-a-Chip," Santa Barbara, CA, 2001 (6 pages).
SM	3R	Silas, Isic, Igor Frumkin, Eilon Hazan, Ehud Mor, and Genadiy Zobin, "System-Level Validation of the Intel Pentium M Processor," Intel Technology Journal, Vol. 7, Issue 02, May 2003 (pages 37-43).
SM	3S	Singh, Virendra, Michiko Inoue, Kewal K. Saluja, and Hideo Fujiwara, "Software-Based Delay Fault Testing of Processor Cores" (10 pages).

<b>EXAMINER</b> Suresh Memula	<b>DATE CONSIDERED</b> 3/10/2006
----------------------------------	-------------------------------------

## PATENT APPLICATION

Sheet 4 of 5

FORM PTO-1449  LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)	ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
	200209677-1	10/759867	
	APPLICANT		
	Elias Gedamu		
	FILING DATE	GROUP	
	1/15/2004	2825	

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
SM	4A	5,590,134	12/31/1996	Yin	
SM	4B	5,581,491	12/3/1996	Biwer et al.	
SM	4C	5,566,344	10/15/1996	Hall et al.	
SM	4D	5,487,169	1/23/1996	Vraney et al.	
SM	4E	5,444,716	8/22/1995	Jarwala et al.	
SM	4F	5,359,547	10/25/1994	Cummins et al.	
SM	4G	5,355,369	10/11/1994	Greenberger et al.	
SM	4H	5,233,612	8/3/1993	Huyskens et al.	
SM	4I	5,157,781	10/20/1992	Harwood et al.	
SM	4J	5,142,688	8/25/1992	Harwood, III	
SM	4K	5,128,737	7/7/1992	van der Have	

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	4L					
	4M					
	4N					
	4O					
	4P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

SM	4Q	Ur, Shmuel and Yoav Yadin, "Coverage Driven Processor Test Generation: Proof of Concept," September 1997 (pages 1-16).
SM	4R	Kim, Hyungwon and John P. Hayes, "High-Coverage ATPG for Datapath Circuits with Unimplemented Blocks," Ann Arbor, MI (10 pages).
SM	4S	

EXAMINER

Suresh Memula

DATE CONSIDERED

3/10/2006

## PATENT APPLICATION

Sheet 5 of 5

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR  
APPLICANT'S INFORMATION DISCLOSURE  
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

200209677-1

APPLICATION NO.

10/759867

CONFIRMATION NO.

APPLICANT

Elias Gedamu

FILING DATE

1/15/2004

GROUP

2825

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
SM	5A	5,119,379	6/2/1992	Dara	
SM	5B	5,067,129	11/19/1991	Evans et al.	
SM	5C	5,021,997	6/4/1991	Archie et al.	
SM	5D	4,707,848	11/17/1987	Durston et al.	
SM	5E	4,520,440	5/28/1985	Buonomo et al.	
	5F				
	5G				
	5H				
	5I				
	5J				
	5K				

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	5L					
	5M					
	5N					
	5O					
	5P					

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	5Q	
	5R	
	5S	

EXAMINER

Suresh Menula *SM*

DATE CONSIDERED

3/10/2006